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Shawn Gettemy

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WAGNER, MURABITO & HAO LLP

Third Floor

Two North Market Street

San Jose, CA 95113

EXAMINER

WANG, JIN CHENG

ART UNIT

PAPER NUMBER

2672

12

DATE MAILED: 05/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

**Application No.**

09/724,197

**Applicant(s)**

GETTEMY ET AL.

**Examiner**

Jin-Cheng Wang

**Art Unit**

2672

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 April 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>10</u> . | 6) <input type="checkbox"/> Other: _____  |

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## DETAILED ACTION

### Response to Amendment

1. The amendment filed on 4/19/2004 has been entered. Claims 1-23 are pending in the application.

### *Claim Rejections - 35 USC § 103*

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla).

4. Claim 1:

(1) Matsuzaki teaches a display unit (e.g., figures 1-2) comprising:

a display panel comprising a pixel matrix comprising: an (m \* n) pixel display memory window region; and an x pixel border region for only displaying a display attribute (e.g., figures 6-7B), wherein said border region surrounds said display memory window region (e.g., figures 6-7B; column 5, lines 25-60);

a memory for containing image data for generating an image within said display memory window region (figures 6-7B; column 5, lines 25-60);

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a display controller (e.g., the display control circuit, SVGA 21 of figure 3) coupled to said memory (e.g., VRAM 22), coupled to receive said display attribute from said border attribute register (e.g., the border producing circuit or registers of figures 1-3; column 5, lines 5-60; column 7, lines 10-65), and coupled to control said display panel (figures 1-7B; column 5, lines 5-60), said display controller for generating a first set of signals (i.e., pixel data) for rendering said image within said display memory window region and for generating a second set of signals (i.e., border pixel data) for display said display attribute within said border region (e.g., column 3, lines 6-25; column 7, lines 5-67; column 8, lines 1-35; column 13, lines 48-60).

(2) However, it is not clear whether Matsuzaki implicitly teaches a frame buffer. It is also not clear whether Matsuzaki teaches a display attribute being selected to provide viewing contrast with image data located near the border region.

(3) Kim teaches implicitly a frame buffer (See Kim column 8, lines 55-67). Furthermore, Singla teaches a display attribute being selected to provide viewing contrast with image data located near the border region (e.g., Singla column 3, lines 28-50; column 5, lines 45-60).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Kim's frame buffer and Singla's border region attribute setting method into Matsuzaki's display unit because Matsuzaki teaches a VRAM for storing image data (Matsuzaki column 2, lines 10-15) and a graphics control circuit fetching pixel data from VRAM 22 (Matsuzaki figures 1-3; column 6, lines 3-65) while Kim teaches a VRAM corresponds to a frame buffer memory (region). Moreover, Matsuzaki teaches selecting/switching one of the display formats (Matsuzaki column 2); setting the format of the binary border pixel data in color bits different from the effective display region (Matsuzaki column 3 and 6) and the format of the synthesized pixel data

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in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the pixel data from the binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6-7) and therefore the claimed limitation suggests an obvious modification of Matsuzaki.

(5) One having the ordinary skill in the art would have been motivated to incorporate the frame buffer of Kim because Kim teaches that the video frame buffer memory is constructed from VRAM (See Kim column 8, lines 55-67). One of the ordinary skill in the art would have been motivated to incorporate Singla's border region attribute setting method because Singla teaches a set of registers associated with a timing generator programmed to a particular resolution (selectable resolution; Singla the Abstract column 5) and Singla further teaches border data set by a solid single-color surrounding the frame buffer image (changeable color; Singla column 8) and a display controller for user-selectable overriding of the predetermined border scheme (changeable attributes; e.g., Singla the Abstract and column 10).

5. Claim 2-4, 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim), Hannah U.S. Patent No. 5,038,297 (hereinafter Hannah) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereinafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla).

6. Claim 2-4, 7, 8:

(1) The claim 2-4, 7,8 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of (1) the second set of signals being generated within invalid timing

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windows with respect to the frame buffer region; (2) a first portion of the second set of signals being generated  $x$  clock cycles before valid data for the frame buffer region commences and a second portion of the second set of signals being generated in an invalid horizontal timing window that ends  $x$  clock cycles after valid data for the frame buffer region; (3) a third portion of the second set of signals being generated in an invalid vertical timing window that commences  $x$  horizontal pulses before a first valid horizontal line commences of a frame and a fourth portion of the second set of signals being generated in an invalid vertical timing window that ends  $x$  horizontal pulses after the end of the last valid horizontal line of the frame; (4)  $x$  being equal 2; (5) the frame buffer region comprising 160 rows and 160 columns of pixels.

As shown in the rejection of claim 1, Matsuzaki/Kim/Hannah/Singla teaches the claimed invention of a display unit.

(2) However, it remains to be shown that Matsuzaki/Kim/Hannah/Singla implicitly teaches the additional claimed limitation as recited in claims 2-4.

(3) Singla, Ogawa and Yuri teaches the additional claimed limitation as recited in claims 2-4. Namely, Singla, Ogawa and Yuri teach the claimed limitation of (1) the second set of signals being generated within invalid timing windows with respect to the frame buffer region (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9; Yuri figure 7); (2) a first portion of the second set of signals being generated  $x$  clock cycles before valid data for the frame buffer region commences and a second portion of the second set of signals being generated in an invalid horizontal timing window that ends  $x$  clock cycles after valid data for the frame buffer region (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9; Yuri figure 7); (3) a third portion of the second set of signals being generated

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in an invalid vertical timing window that commences x horizontal pulses before a first valid horizontal line commences of a frame and a forth portion of the second set of signals being generated in an invalid vertical timing window that ends x horizontal pulses after the end of the last valid horizontal line of the frame (Singla figures 2-5; Ogawa column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9); 4) x being equal 2 (Ogawa figure 7; Singla figure 2; Yuri figure 7); (5) the frame buffer region comprising 160 rows and 160 columns of pixels (Ogawa figure 7; Singla figure 2; Yuri figure 7).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated Singla, Ogawa and Yuri's timing generator into Matsuzaki/Kim/Hannah/Yuri/Singla's display device because Matsuzaki suggests partial rewrite driving using display start line address, the number of continuous display lines, the total number of lines, the total number of pixels, and the border region to the line address producing circuit, thereby obtaining partial display information (Matsuzaki column 8, lines 1-67). Matsuzaki discloses a plurality of display formats for the effective display region (Matsuzaki column 8, lines 1-67). Therefore the claimed limitation suggests an obvious modification of Matsuzaki/Kim/Hannah/Yuri/Singla.

(5) One having the ordinary skill in the art would have been motivated to do this because Ogawa teaches timing chart for the horizontal/vertical timing intervals to generate the timing signals so that the input image signal is displayed in the center and its periphery is made a frame, the drive of picture elements corresponding to the frame can be carried out during the horizontal/vertical blanking intervals (Ogawa column 5, lines 4-67; column 6, lines 1-67; Yuri figure 7).

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7. Claim 5, 6, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Hannah U.S. Patent No. 5,038,297 (hereinafter Hannah); Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla).

Claim 5:

The claim 5 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the display attribute of the border region comprising a color attribute and an intensity attribute. However, Matsuzaki further discloses the claimed limitation of the display attribute of the border region comprising a color attribute and an intensity attribute (e.g., Matsuzaki figures 6-8).

Claim 6:

The claim 6 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the display panel being a thin film transistor liquid crystal display panel. However, Matsuzaki further discloses the claimed limitation of the display panel being a thin film transistor liquid crystal display panel (e.g., Matsuzaki column 1, lines 20-60; column 5, lines 1-25).

Claim 9:



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The claim 9 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of background display attribute register. Matsuzaki further discloses the claimed limitation of background display attribute register (e.g., Matsuzaki figures 6-8).

8. Claims 10-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of in view of Kim et al. U.S. Patent No. 5,355,443 (hereafter Kim) and Hannah U.S. Patent No. 5,038,297 (Hannah), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla).

9. Claim 10:

The claim 10 encompasses the same scope of invention as that of claims 1 and 2. The claim 10 is rejected for the same reasons set forth in claims 1 and 2.

Claims 11-12:

The claim 11, or 12 encompasses the same scope of invention as that of claims 1-4. The claim 11 is rejected for the same reasons set forth in claims 1-4.

Claim 13:

The claim 13 encompasses the same scope of invention as that of claims 1-5. The claim 13 is rejected for the same reasons set forth in claims 1-5.

Claim 14:

The claim 14 encompasses the same scope of invention as that of claims 1-6. The claim 14 is rejected for the same reasons set forth in claims 1-6.

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Claim 15:

The claim 15 encompasses the same scope of invention as that of claims 1-7. The claim 15 is rejected for the same reasons set forth in claims 1-7.

Claim 16:

The claim 16 encompasses the same scope of invention as that of claims 1-8. The claim 16 is rejected for the same reasons set forth in claims 1-8.

Claim 17:

The claim 17 encompasses the same scope of invention as that of claims 1-9. The claim 16 is rejected for the same reasons set forth in claims 1-9.

10. Claims 18-23 are rejected under 35 U.S.C. 103(a) as being as being unpatentable over Matsuzaki et al. U.S. Pat. No. 6,140,992 (hereinafter Matsuzaki), in view of in view of Kim et al. U.S. Patent No. 5,355,443 (hereinafter Kim) and Hannah U.S. Patent No. 5,038,297 (hereinafter Hannah) and Yuri et al. U.S. Patent No. 5,805,149 (hereinafter Yuri), further in view of Ogawa et al. U.S. Patent No. 6,018,331 (hereafter Ogawa) and Singla et al. U.S. Patent No. 6,597,373 (hereinafter Singla) and He et al. U.S. Patent No. 6,323,849 (He).

Claims 18-23:

The claim 18-23 encompasses the same scope of invention as that of claims 1-9 except additional claimed limitation of a portable electronic device. However, He/Yuri further discloses the additional claimed limitation of a portable electronic device (He column 1, lines 20-35; Yuki column 14, lines 1-15).

*Remarks*

11. Applicant's arguments, filed 04/19/2004, paper number 11, have been fully considered but they are not deemed to be persuasive.

12. Applicant argues in essence with respect to the Claim 1 and similar claims that:

(A) "Applicants respectfully note that the prior art reference, Matsuzaki et al., does not comprise nor suggest a controllable pixel border region that provides viewing contrast.

The Matsuzaki et al. reference discloses a display control system for controlling the display format to be displayed by a display apparatus. As such, the Matsuzaki et al. reference discloses a border section that displays border pixel data to frame a display image frame. However, Applicants respectfully point out the Matsuzaki et al. reference does not comprise or suggest a pixel border region displaying a display attribute that is selected to provide viewing contrast with images and/or characters near the border region, as in embodiments of the present invention as claimed in independent Claims 1, 10, and 18."

In response to the arguments in (A), Matsuzaki teaches selecting/switching one of the display formats (Matsuzaki column 2); setting the format of the binary border pixel data in color bits different from the effective display region (to provide viewing contrast; see Matsuzaki column 3 and 6) and the format of the synthesized pixel data in the border section produced as 8-bit parallel data by the border producing circuit 25 synthesized with the pixel data from the binarizing half tone processing circuit 26 by the synthesizing circuit 27 (Matsuzaki column 3, 6-7). Therefore, Matsuzaki at least suggests a pixel border region displaying a display attribute

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(e.g., color) that is selected to provide viewing contrast (because the color for the border region surrounding the frame buffer region has been changed, the viewing contrast has been altered) with images and/or characters (images and/or characters in the frame buffer region) near the border region. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

13. Applicant argues in essence with respect to the Claim 1 and similar claims that:

(B) “Moreover, the Singla et al. reference fails to remedy the shortcomings of the Matsuzaki et al. reference. Specifically, Applicants respectfully note that the prior art reference, Singla et al., does not comprise nor suggest a controllable pixel border region that provides viewing contrast. In contrast to independent Claims 1, 10, and 18 of embodiments of the present invention, the Singla et al. reference discloses a display controller that is capable of generating image borders based on scanning resolution information. Importantly, the Singla et al. reference determines the appropriate image border based on the resolutions of the image and display device....As such, the Singla et al. reference refers to an x and y border resolution of an image border, and does not comprise nor suggest a pixel border region displaying a display attribute that is selected to provide viewing contrast with images and/or characters near the border region, as in embodiments of the present invention as claimed in independent Claims 1, 10, and 18.”

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In response to the arguments in (B), Singla teaches a display attribute being selected to provide viewing contrast with image data located near the border region (e.g., column 3, lines 28-50).

Singla teaches a border region attribute setting method in which a set of registers associated with a timing generator is programmed to a particular resolution (selectable resolution; Singla the Abstract column 5). Singla further teaches border data set by a solid single-color surrounding the frame buffer image (changeable color; Singla column 8) and a display controller for user-selectable overriding of the predetermined border scheme (changeable attributes; e.g., Singla the Abstract and column 10). Therefore, Singla teaches the claim limitation of a pixel border region displaying a display attribute (such a resolution and color settable by the programmable registers) that is selected (selectable color and resolution) to provide viewing contrast (viewing contrast to the frame buffer area is changed because the display attributes surrounding the frame buffer area has been change due to the controllable change of color and resolution of the border area) with images and/or characters near the border region. The color and resolution change of the border area provides the viewing contrast of the frame buffer region in the display.

14. Applicant argues in essence with respect to the Dependent Claims 2-4 and similar claims that:

(C) "As to Claims 2-4, Applicants respectfully contend that the prior art references do not comprise, suggest, or disclose a second set of signals being generated within invalid timing windows with respect to the frame buffer region, wherein the second set of signals are for displaying the display attribute for viewing contrast within the border region. In particular, each of the prior art references, Singla et al., Ogawa, and Yuki et al., disclose

the generation of a second set of signals within blanking timing windows, etc. for display within a frame buffer region that is designated as a border to an image. That is, in each of the prior art references, border data is generated for display within the frame buffer. As such, in each of the prior art references, pixels designated as a border at one time in the frame buffer region, can be designated as a displaying image data at another time in the frame buffer region...pixels in the frame buffer region are for displaying images, and pixels in the x-pixel border region are for only displaying border attribute data, and never image data.”

In response to the arguments in (C), the Examiner asserts that Applicant’s statement is incorrect that, in each of the prior art references, pixels designated as a border at one time in the frame buffer region, can be designated as a displaying image data at another time in the frame buffer region. Ogawa teaches, in column 5, lines 4-67; column 6, lines 1-67; Ogawa figures 7-9 the claimed limitation of the second set of signals being generated within invalid timing windows with respect to the frame buffer region. Specifically, Ogawa teaches timing chart for the horizontal/vertical timing intervals to generate the timing signals so that the input image signal is displayed in the center and its periphery is made a frame, the drive of picture elements corresponding to the frame can be carried out during the horizontal/vertical blanking intervals (Ogawa column 5, lines 4-67; column 6, lines 1-67). In view of the timing chart in conjunction with the source driver and enable signal (Ogawa column 5-6), the pixels for the border region can only be displayed in the border region and cannot be displayed as the image data in the frame buffer region.

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Applicant further argues that “pixels in the frame buffer region are for displaying images, and pixels in the x-pixel border region are for only displaying border attribute data, and never image data.” However, the Claims 2-4 and 11-12 called for “a second set of signals being generated within invalid timing windows with respect to the frame buffer region, wherein the second set of signals are for displaying the display attribute for viewing contrast within the border region.” The Examiner asserts that the second set of image signals of the cited reference, which is separate from the first set of image signals for displaying in the frame buffer region, meets the claim limitation of “the second set of signals” as set forth in the Claims 2-4 and similar claims. Moreover, the cited reference also teaches setting the attribute for the border area wherein the second set of image signals displayed on the border area as black (the black color attribute) and the pixels in the x-pixel border region are for only display the border attribute data such that the border image pixels are displayed in the black color attribute. Therefore, the cited reference in particular meets the claim limitation of “pixels in the x-pixel border region are for only displaying border attribute data.”

### *Conclusion*

15. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (703) 605-1213. The examiner can normally be reached on 8:00 - 6:30 (Mon-Thu).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jcw



MICHAEL RAZAVI  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600